Calorimeter Assembly and Tests

Bernard Phlips
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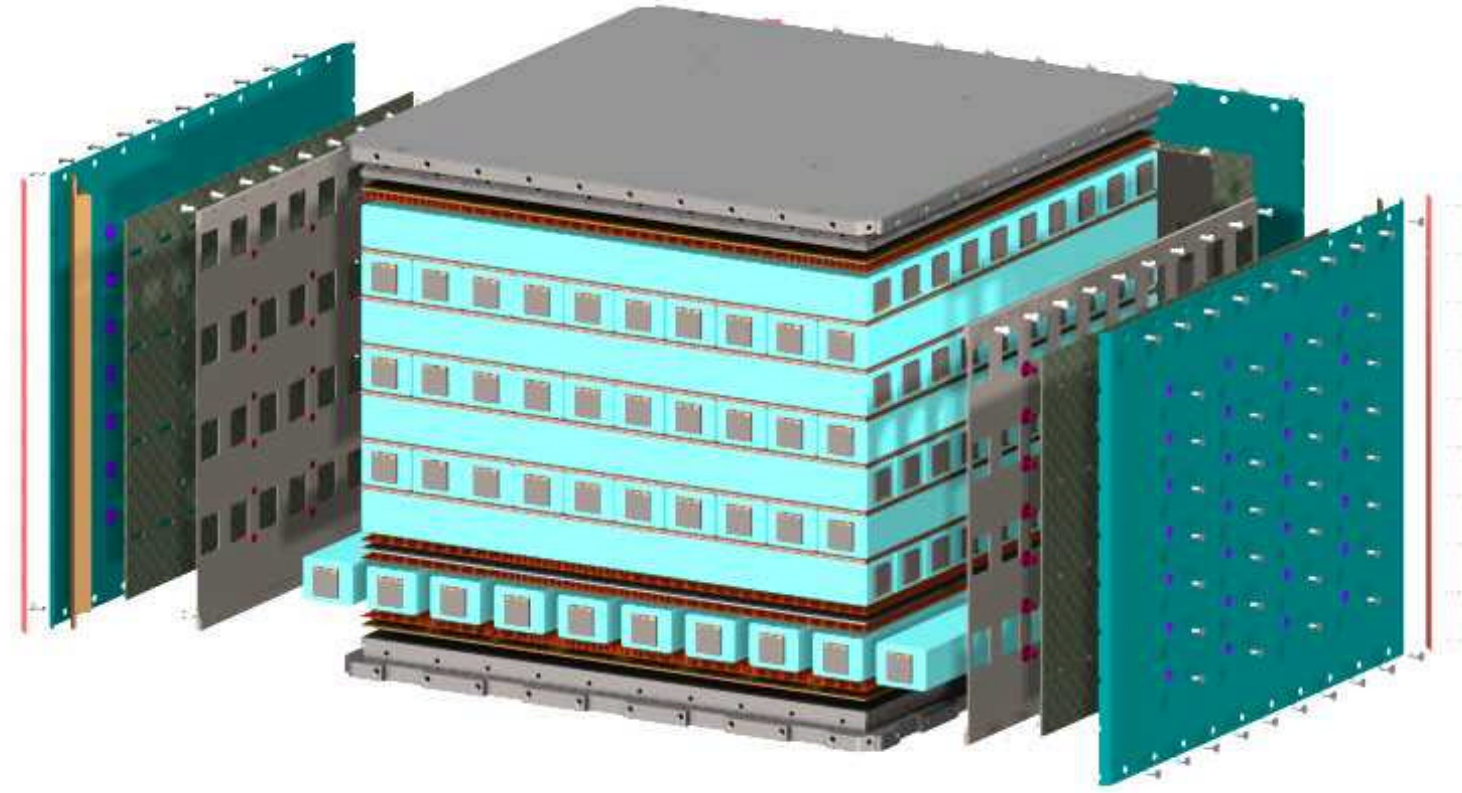
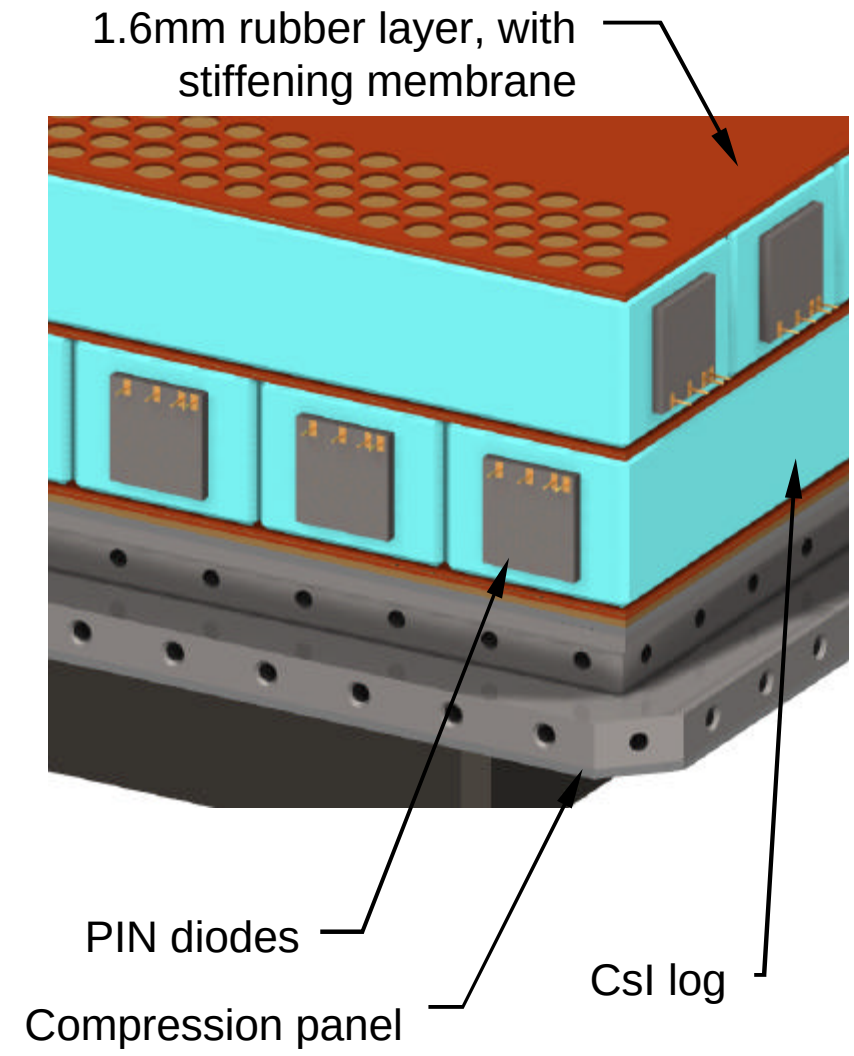
Mechanical Concept

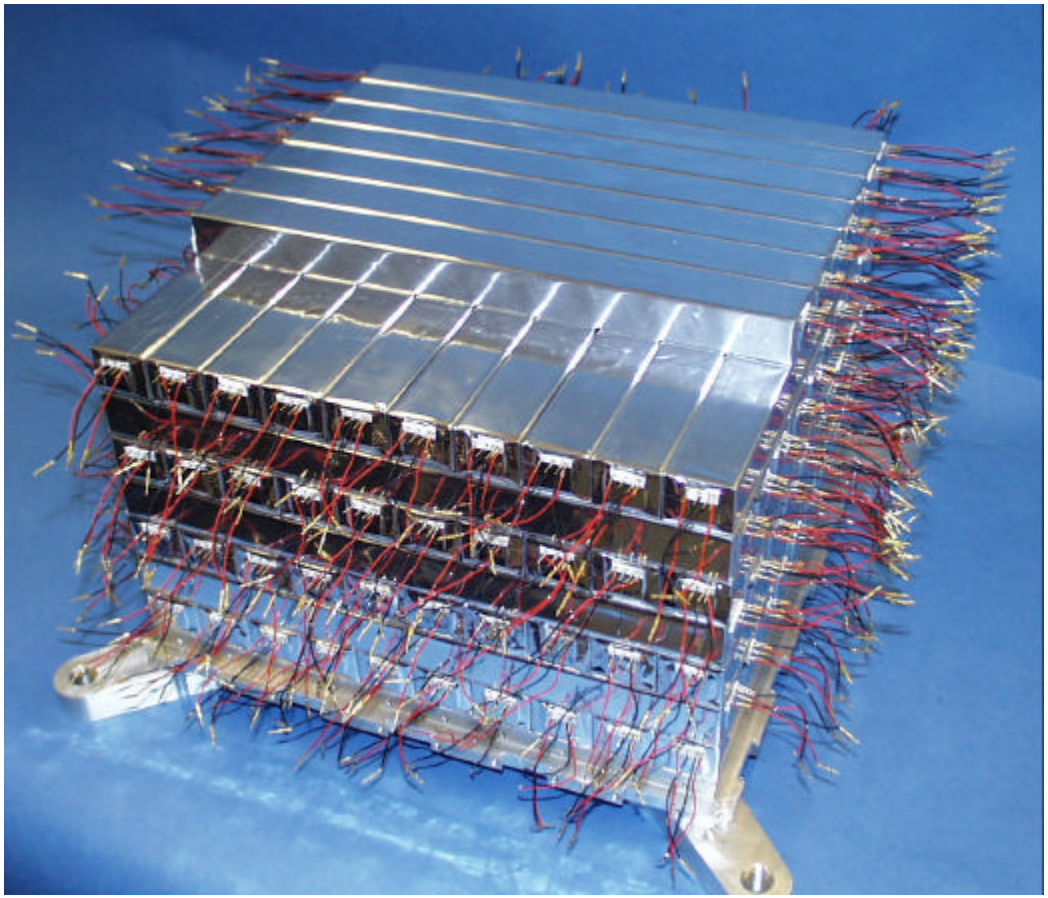


Detail of Concept

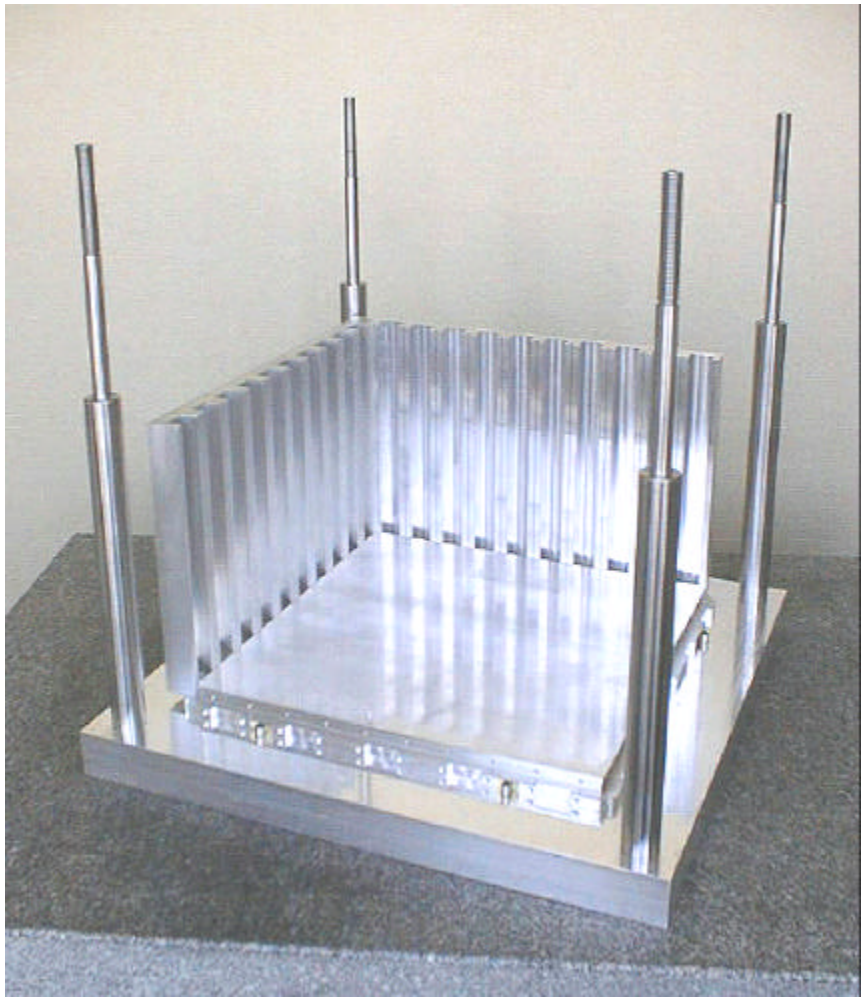


-Top and bottom are honeycomb
with face-sheets
-Inner side-wall holds top and bottom
-Inner side-wall is 1 mm Al
-Outer wall is 1 mm Al
-Electronics is held between
inner and outer side-walls
-Rubber sheet above and below each layer
-Al shim between layers of rubber

Hodoscopic Stacking



Press and Alignment Fixture



-Real Stacking done in press

-Use alignment plates
bolted to base plate

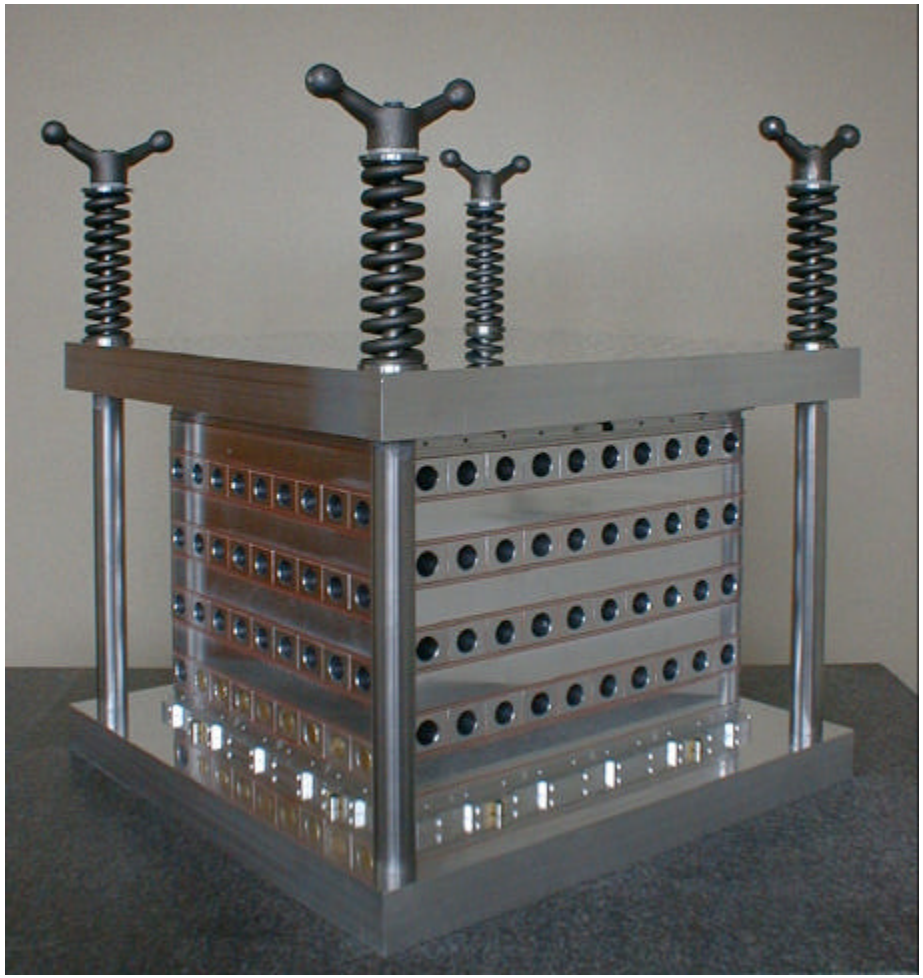
Partial Stacking

-Shim between logs
if needed

-Adjust Al shim as needed

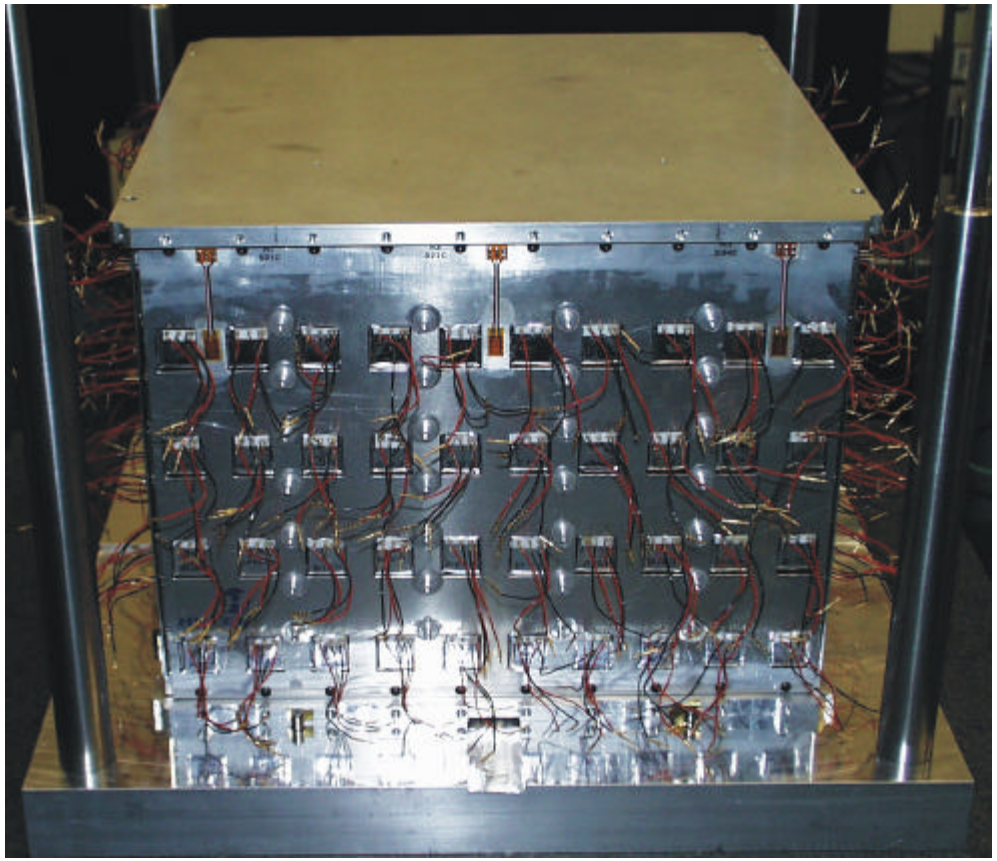
-Process took < 1 day

Loading of Stack



- Compress to desired pressure
- Put on side-walls
- fastened with 10 screws on top and bottom of each wall
- Take off pressure
- Take off top of press

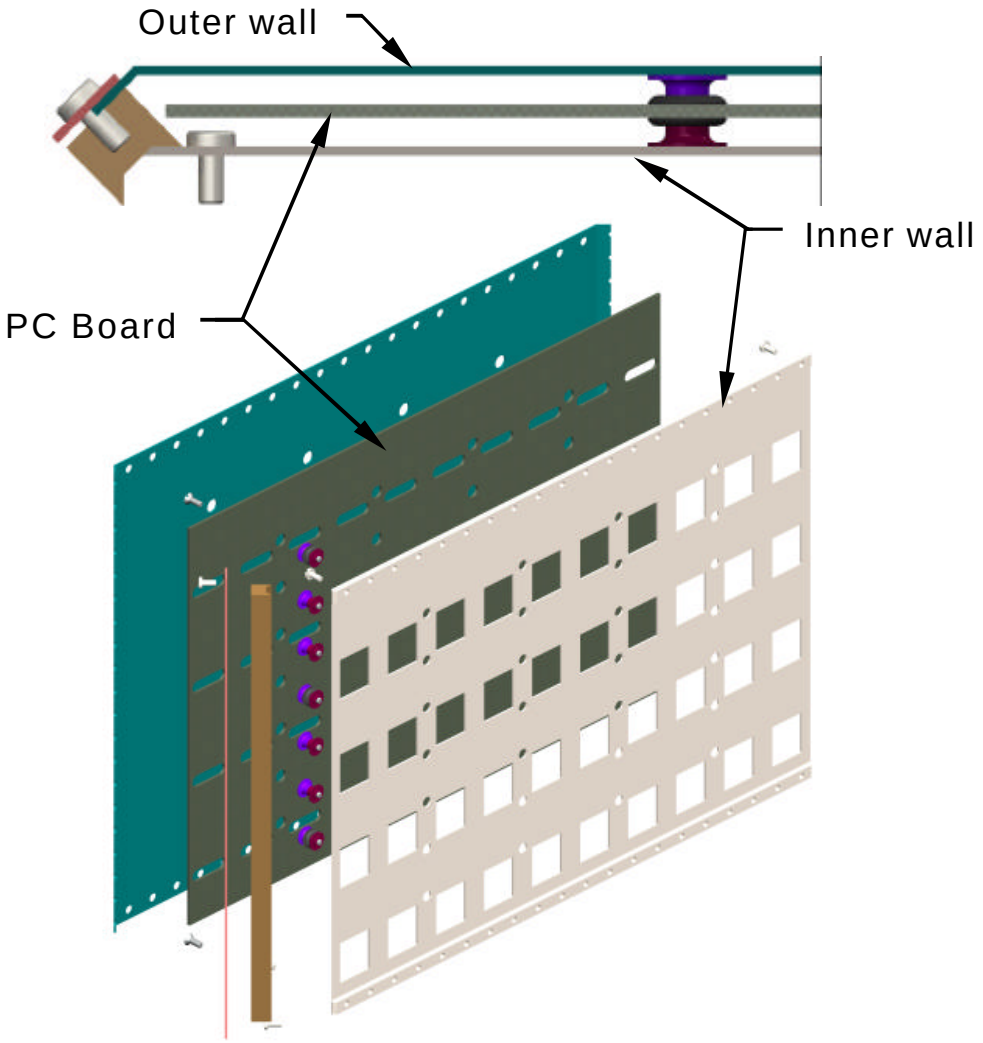
Stack under Compression



-Pin diodes and contacts stick out through Al

-Ready for front end electronics board

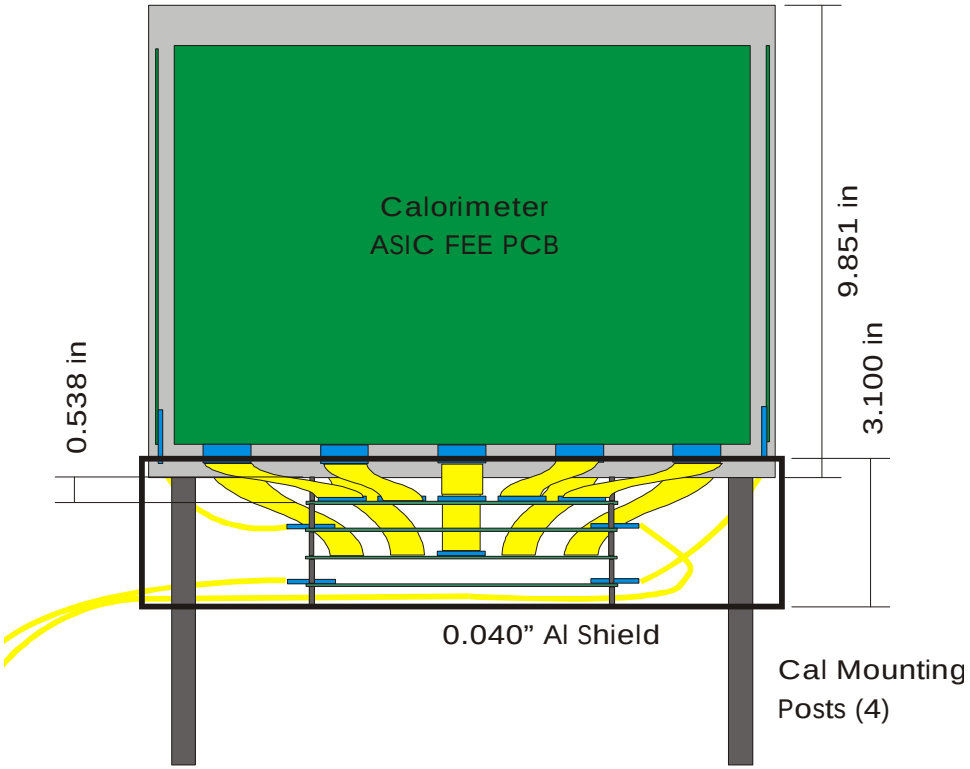
FEE Board Location



- Inner and outer wall connected by posts
- Strengthens assembly
- Could hold entire layer if slipping
- Holds electronics boards
- Shields electronics boards
- Connection between diode and PC board flexible

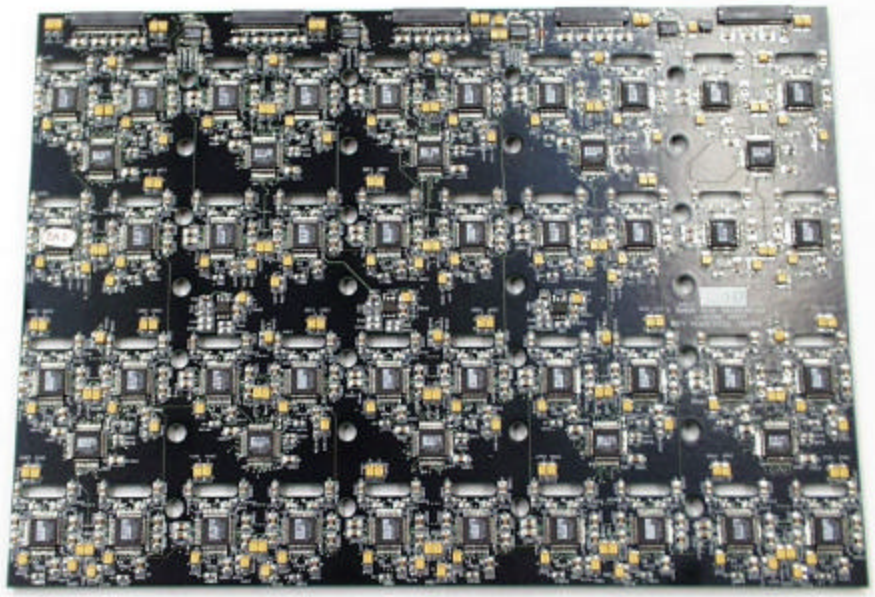
=>de-couple from thermal expansion of CsI crystals

FPGA Board Location



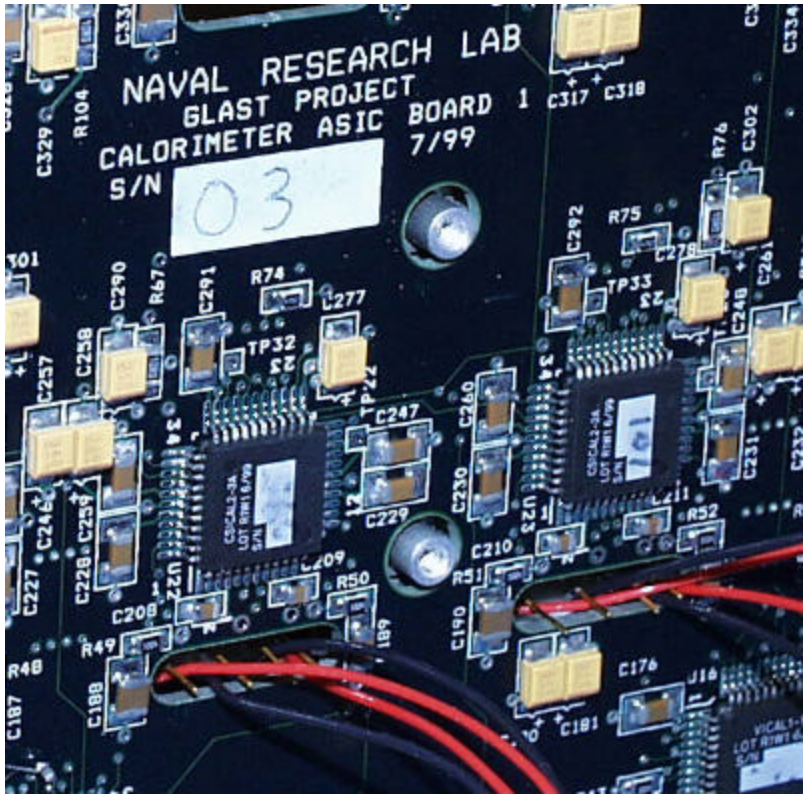
- Need additional board between for FEE board and data acquisition system
-1 FPGA board per side
- all 4 stacked under calorimeter bottom
- diode bias internal (battery)
- only umbilical between calorimeter and DAQ

FEE Board



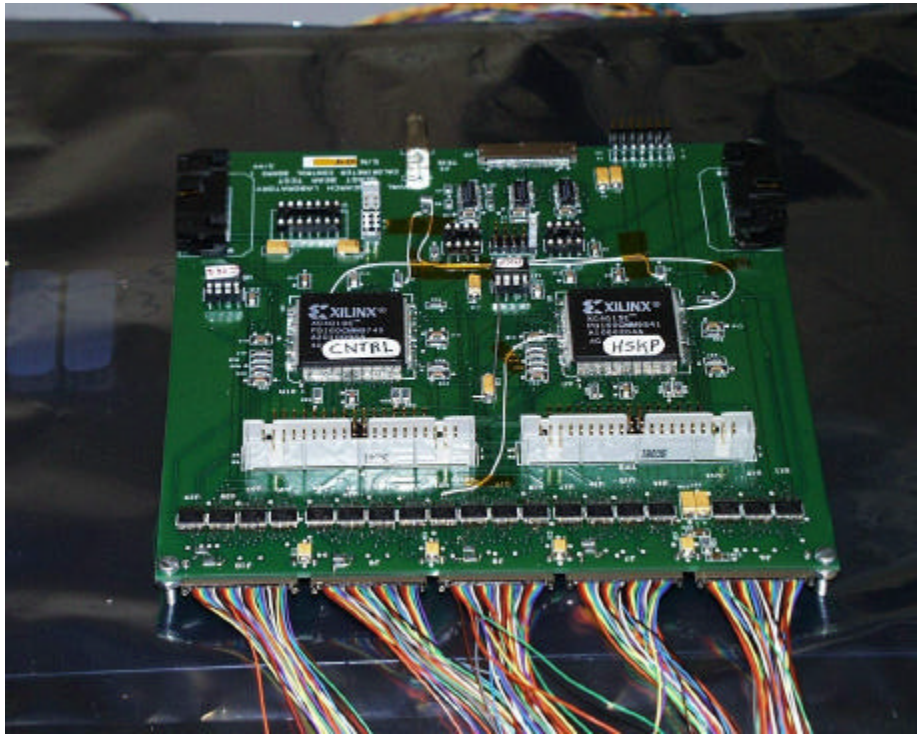
- One board per side
- Supports 40 crystals
- Supports 80 diodes
- Has 40 ASICs with amps
- Has 10 ASICs with V/I
-16 DACs to set levels
- Has 80 preamps
- Has 240 shapers
- Different ADCs in X,Y
-1400 components per board

Holes in FEE Board



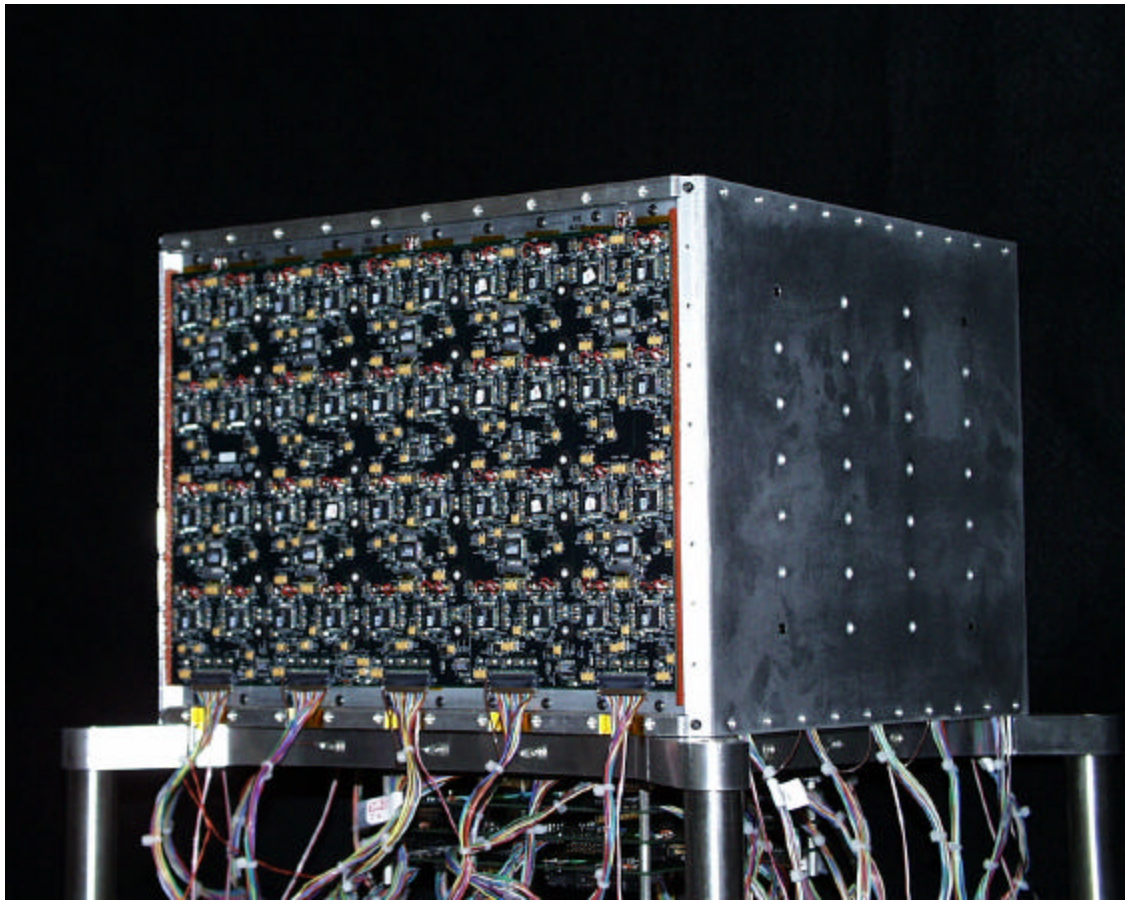
- Holes needed for signals from PIN diode and posts
- Think before choosing orientation of diode on crystal
- Might NOT want mirror image epoxy of diodes on crystal

FPGA board

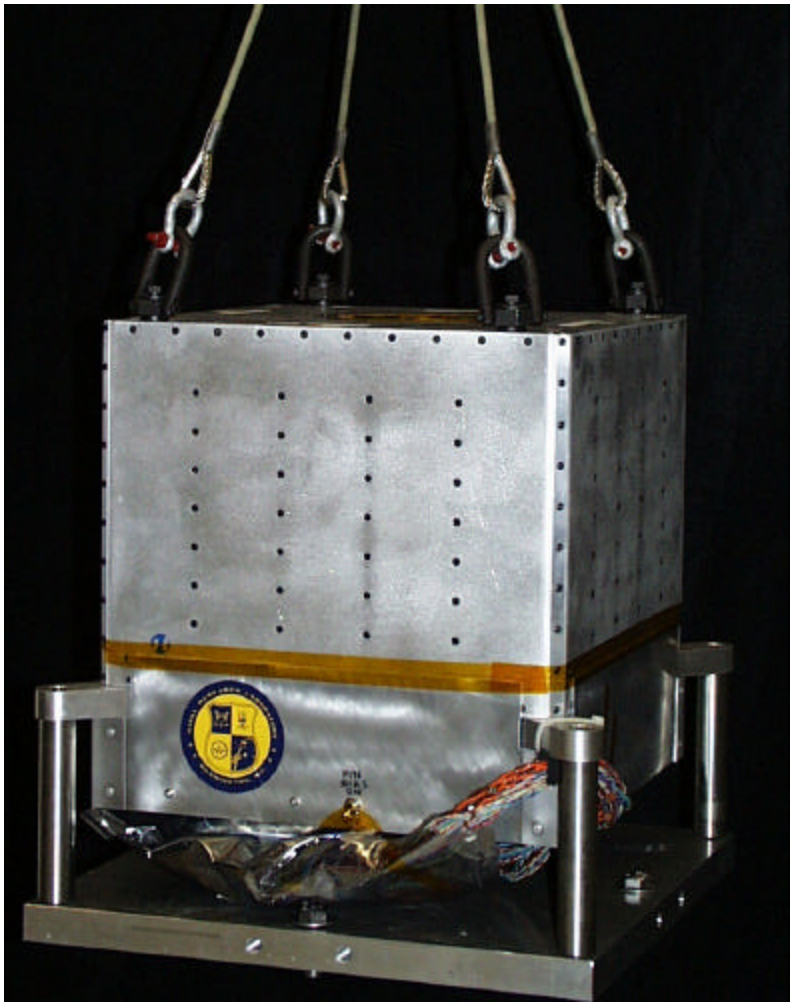


- FPGAs too big for FEE board
- Board has 2 Xilinx FPGAs
- One does data readout
  data formatting
- Other does command
  control
  trigger
  housekeeping
- Might want to keep 2nd board concept for flight

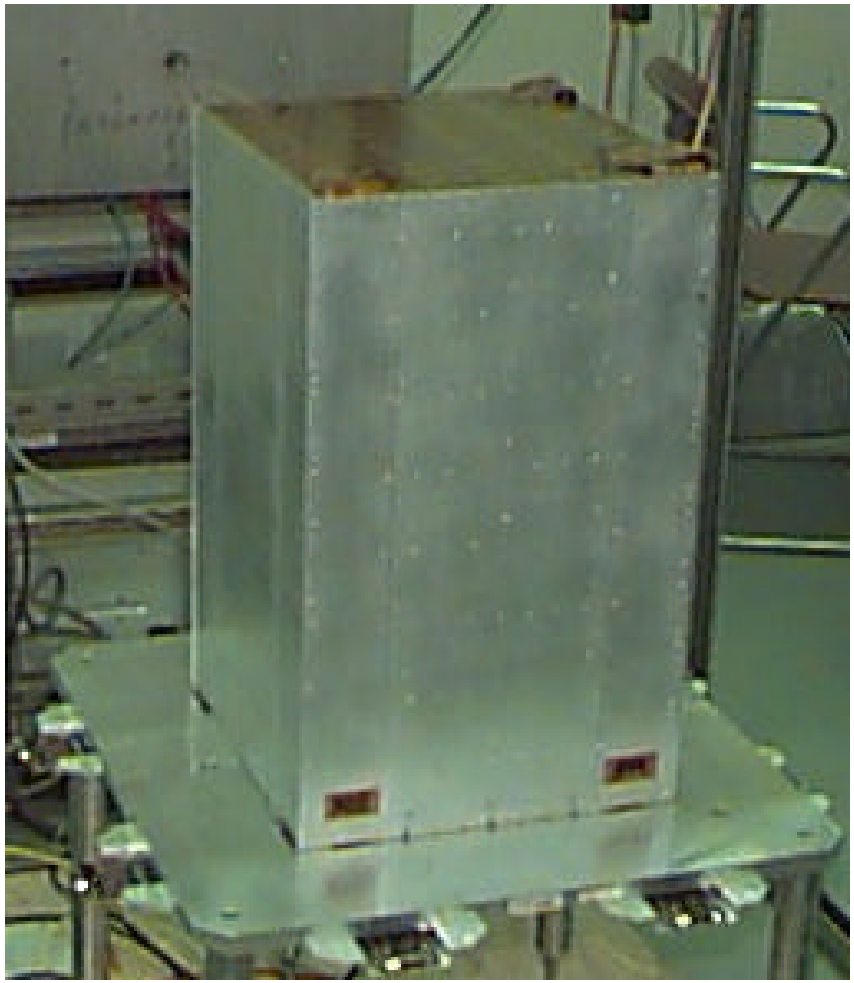
Partially Assembled Calorimeter



Assembled Calorimeter

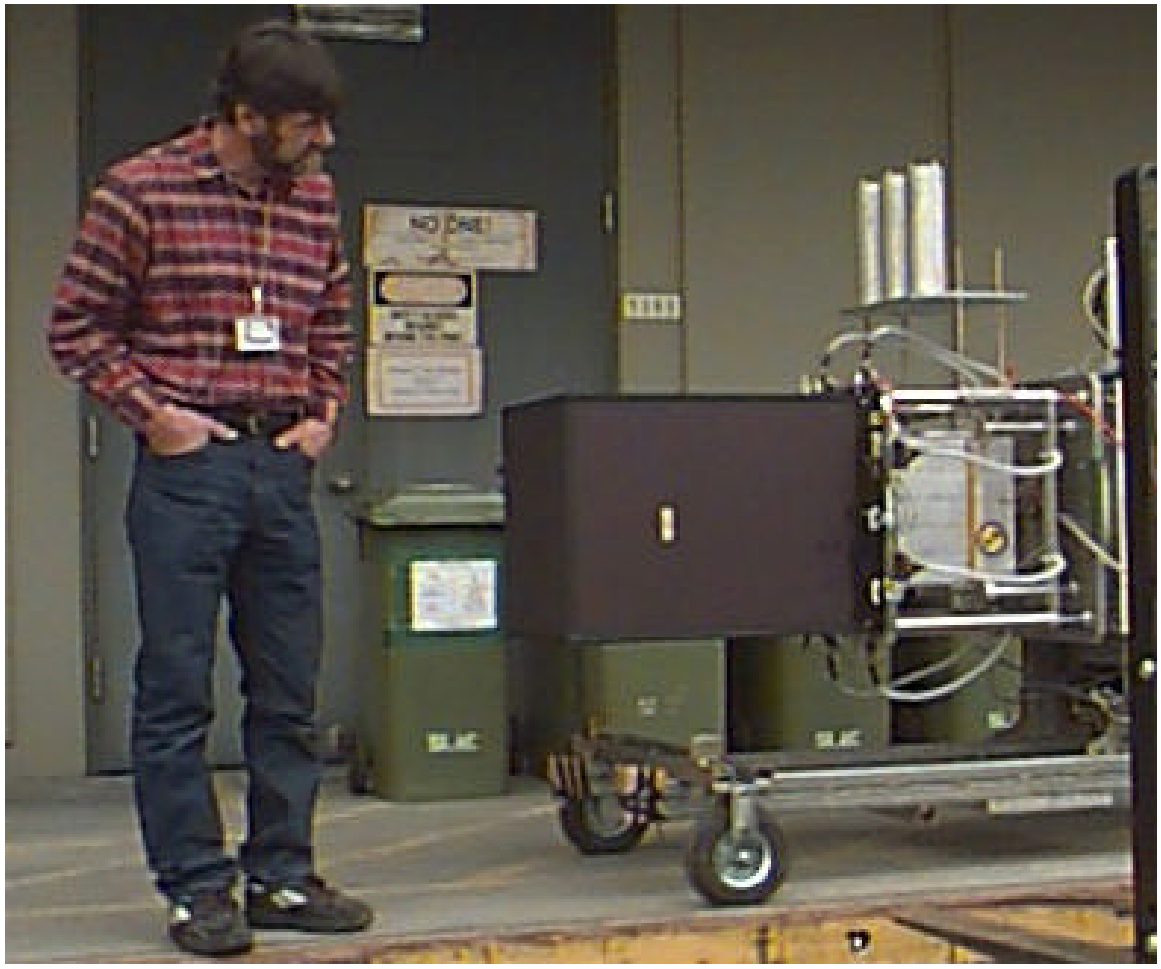


Tracker

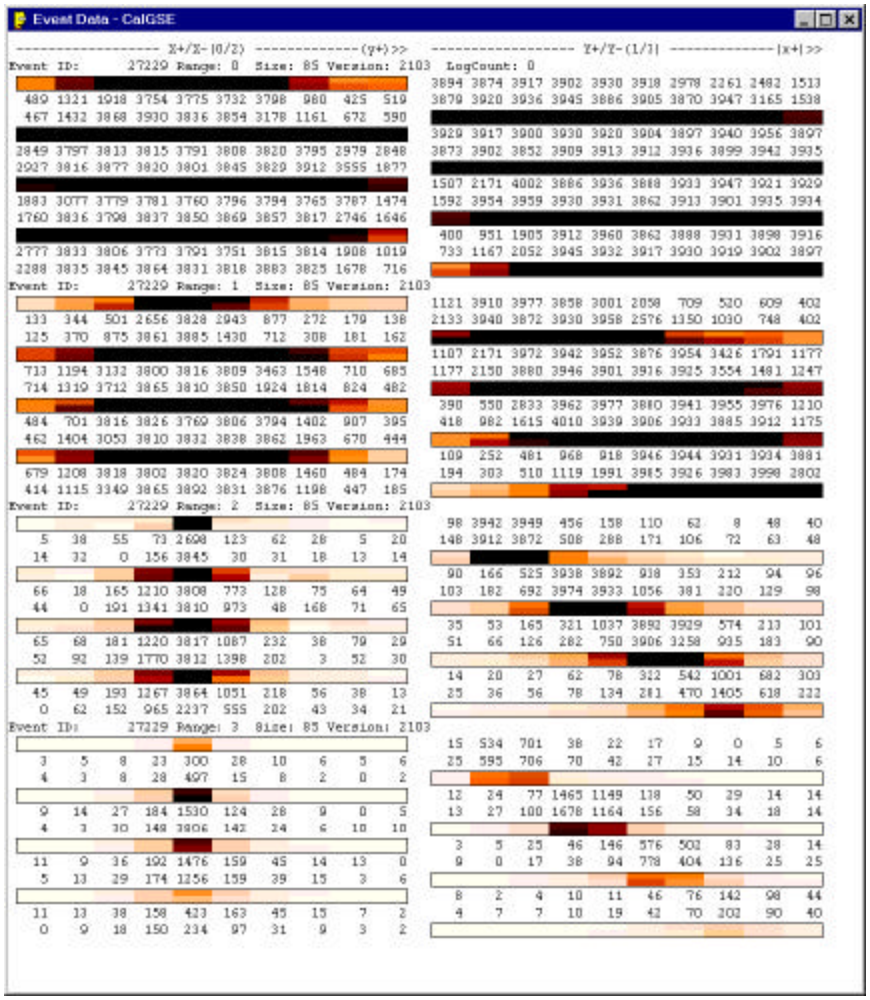


- 16 trays of silicon
  (32 planes of silicon)
- 8 trays fully populated
-mix 4 and 6 inch material
-bottom 2 no Pb converter
-top 10 have 2.5 % Pb
-next 4 have 25% Pb
-200 micron resolution
-~350 micron thick Si

Calorimeter, Tracker and ACD



On-Line Displays

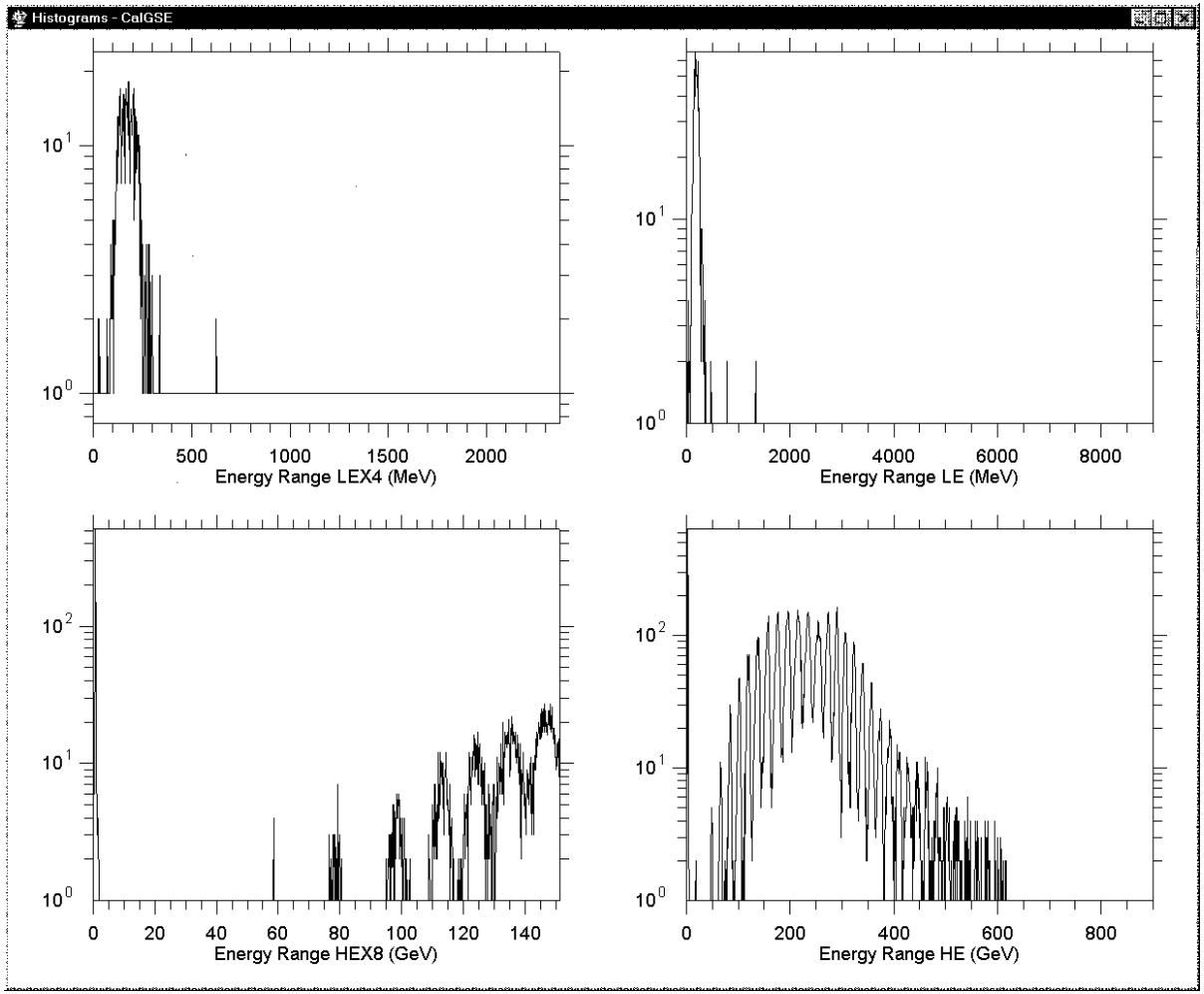


Display one range or all four ranges.

For ~12 positrons in a pulse from 20 GeV beam:

- lowest range saturated
-highest range not saturated
-both ends displayed

Multi-Particle Energy Spectra



Run self-triggered:

-see muons in
low energy range
-see multiplicity of
particles
up to 600 GeV

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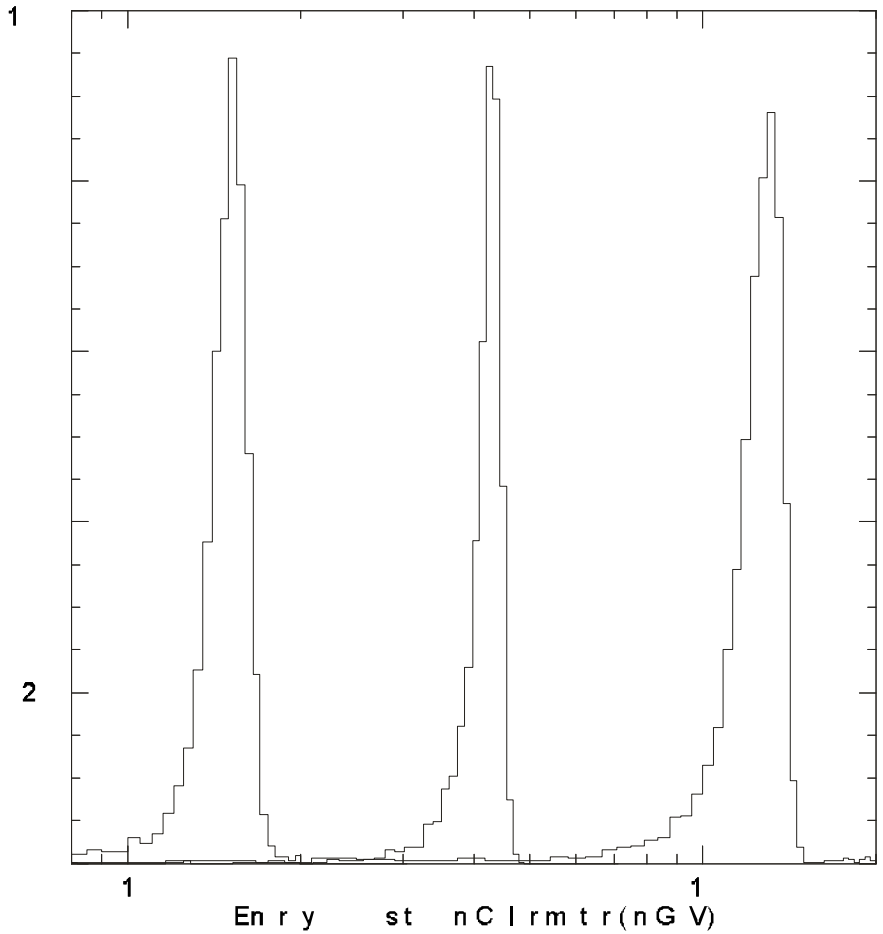
Washington DC

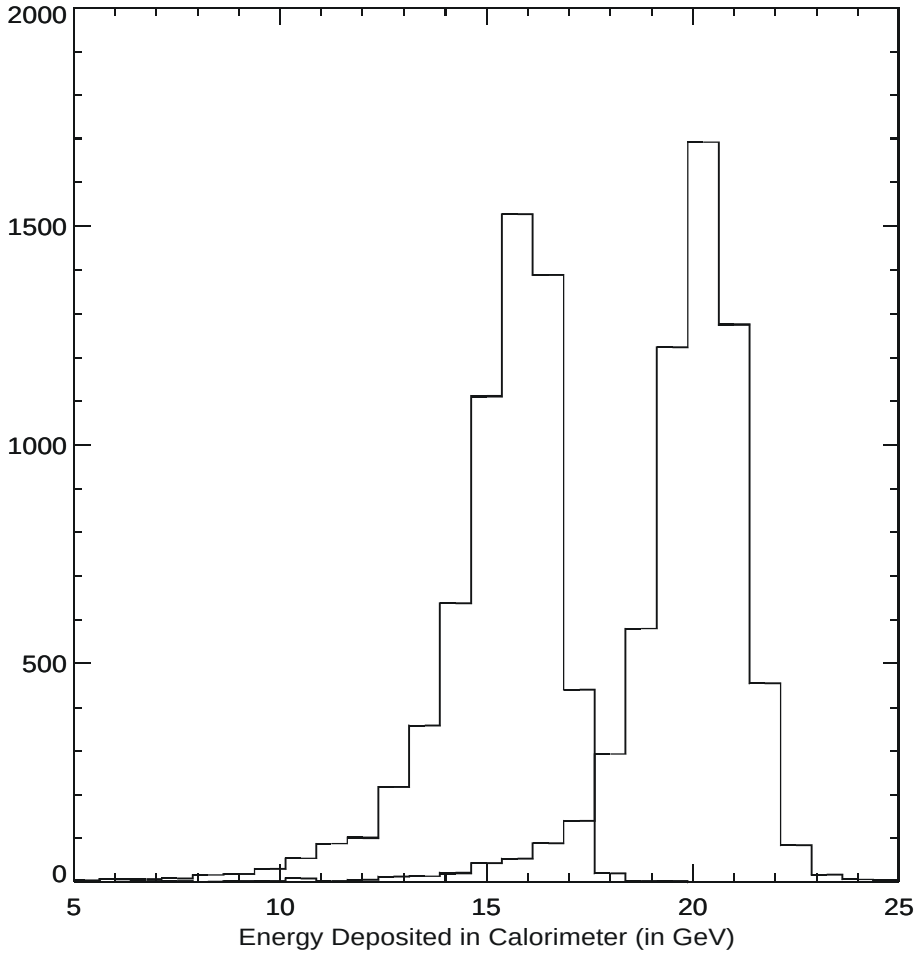
Total Energy



Positron Runs :

- < 1 particle per pulse
- 2 GeV, 5 GeV, 20 GeV beams
- Normal incidence
-Total energy deposited,
not corrected

Corrected Energy

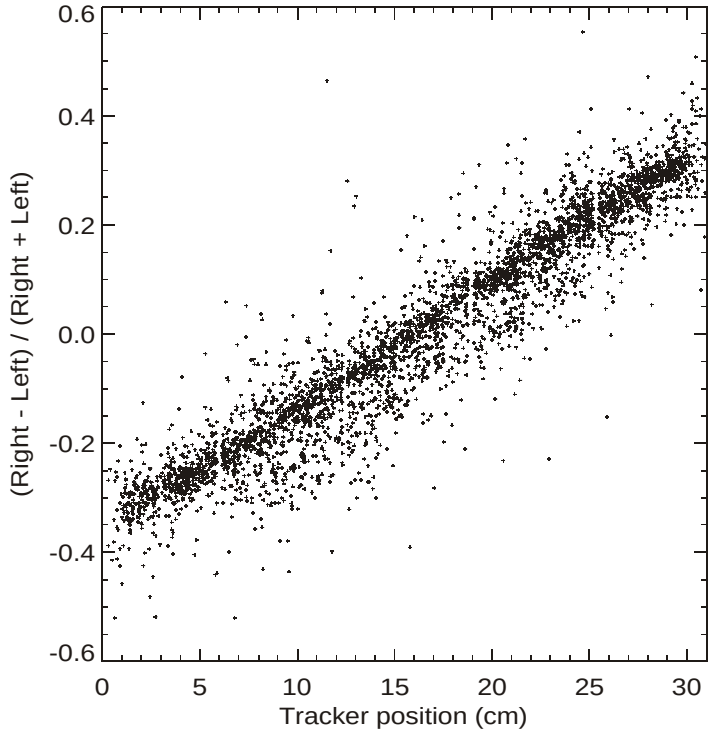


- Fit shower profile
- Derive improved
  energy measurement
- Layer 5 not included
- Will improve with layer 5
- Normal incidence
- All other angles better

Light Tapering

- Mapping the array of CsI bars.
- For example:
  - Beam is 2 GeV e+.
  - 10 runs on 3.1-cm centers.
  - Crystal in 2nd layer from top.
- Light asymmetry map.

  $\Lambda = (R - L) / (R + L)$
  - Slope ~ 2% per cm.
  - Tracker positions:
    - Simple mean of hits in last x,y.
    - Sensitive to outliers.
- Analysis performed on hbooks.



Calorimeter Vibration Tests

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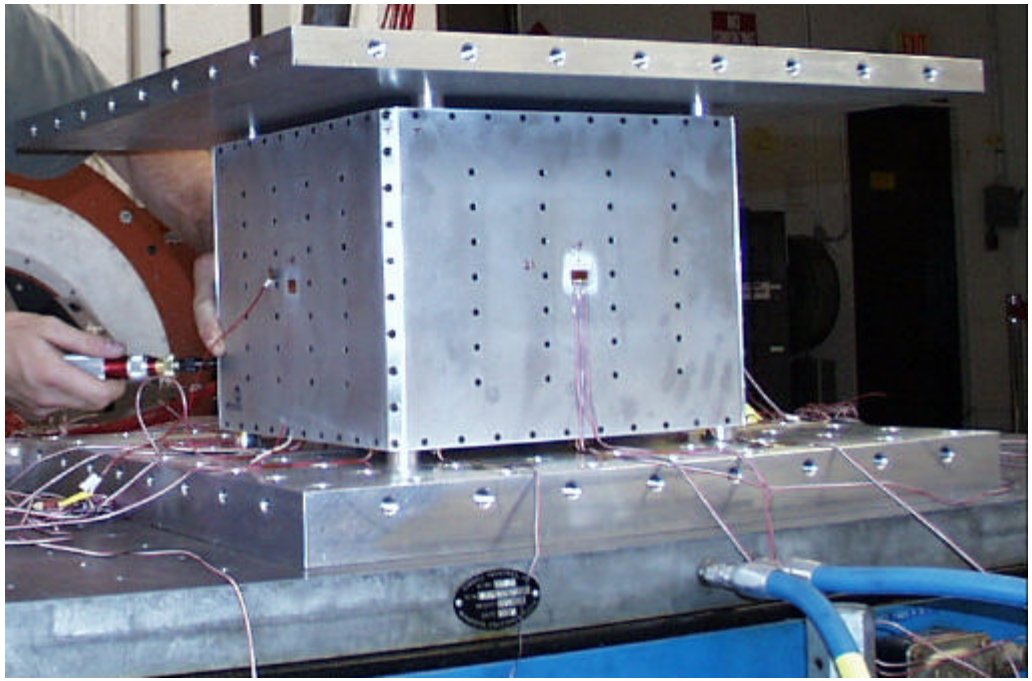
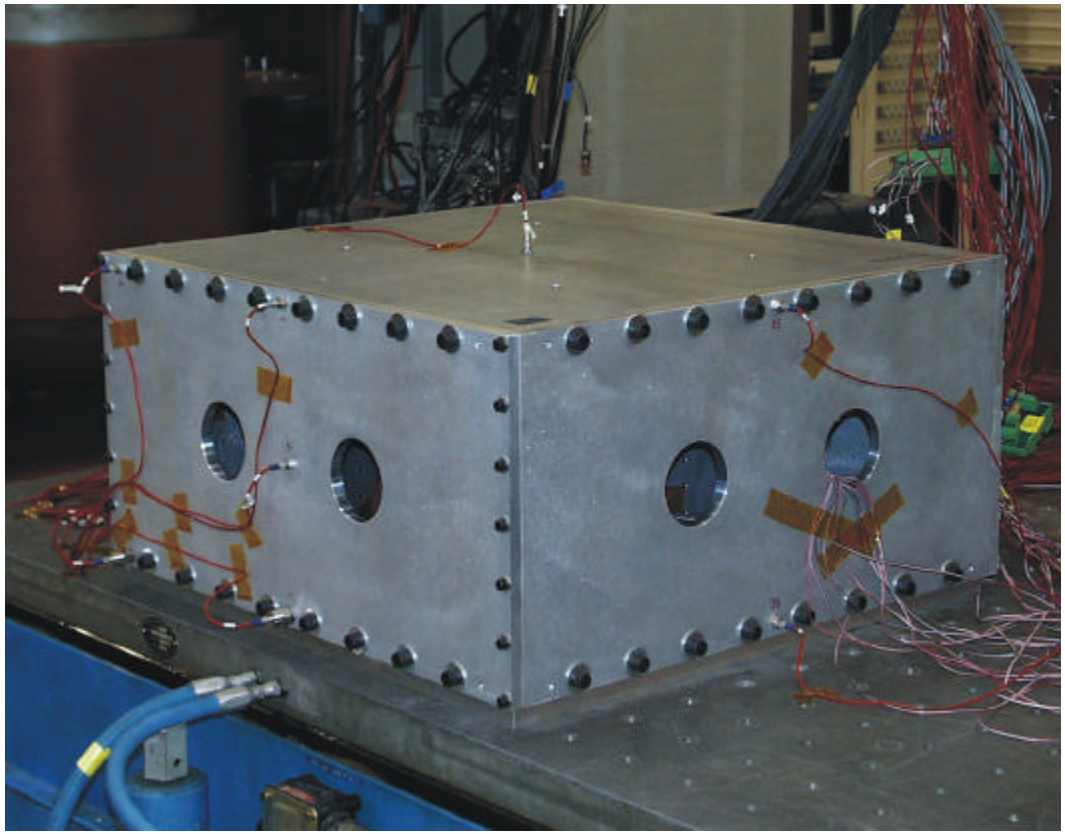
Vibration Test Setup

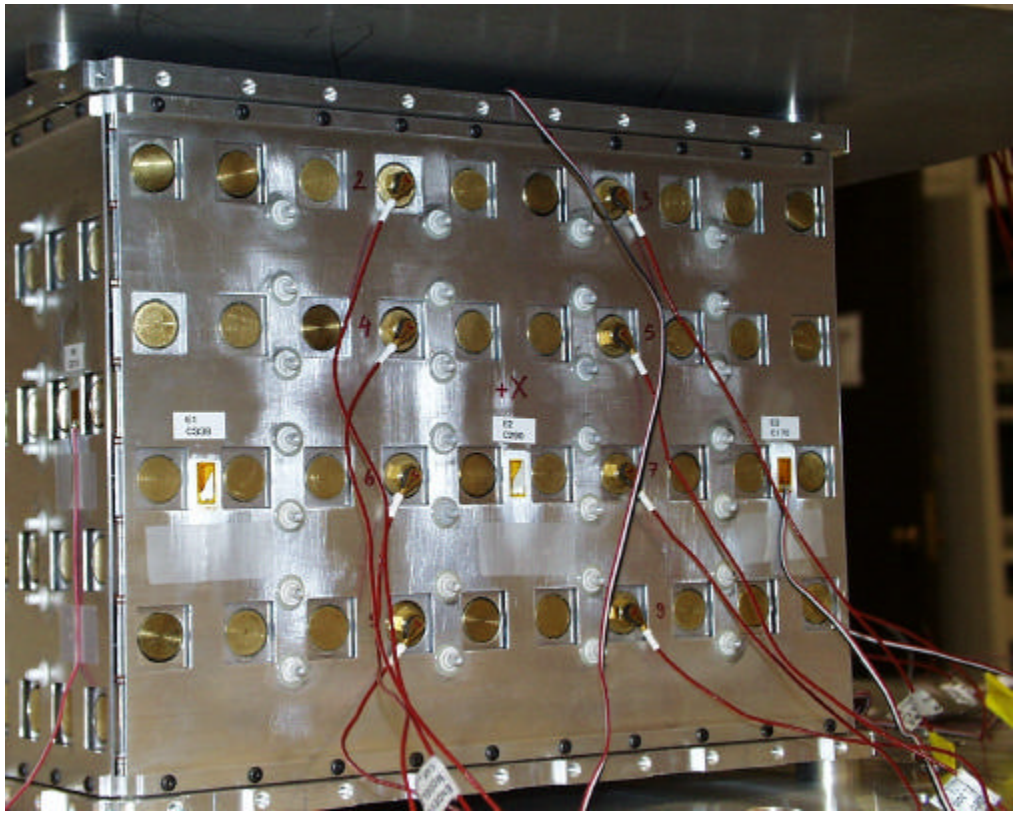


- made copy of calorimeter
- fake logs, real mass
- tests performed at NRL
- used vertical shaker for
  longitudinal tests
- used horizontal shaker
  for transverse tests
- test fixture simulated
  mounting configuration for flight:
  4 points on bottom and
  4 points on top

Test Fixture



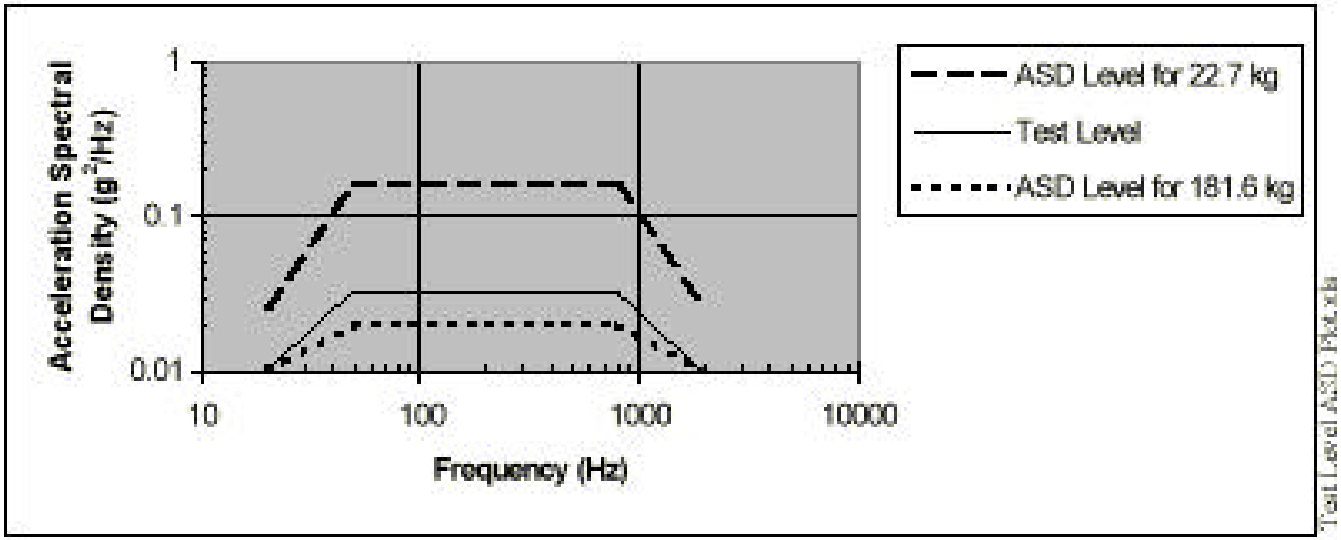
Sensors



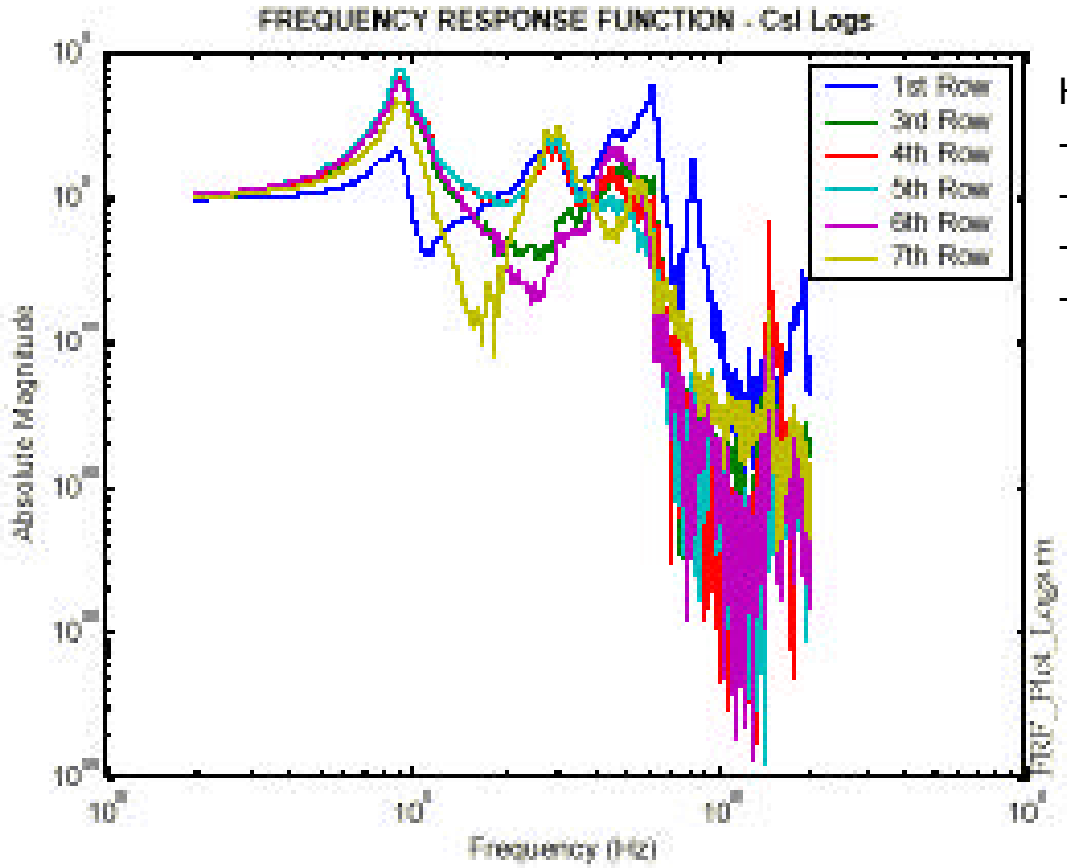
- Used >30 accelerometers
-mounted on: logs
inside walls
outside walls
top plate
fixture

Random Vibration Specifications

Frequency (Hz)	ASD Level (g^2/Hz)
20	0.01
20 to 50	+3.92 dB/oct
50 to 800	0.033
800 to 2000	-3.92 dB/oct
2000	0.01
6.81 grms	

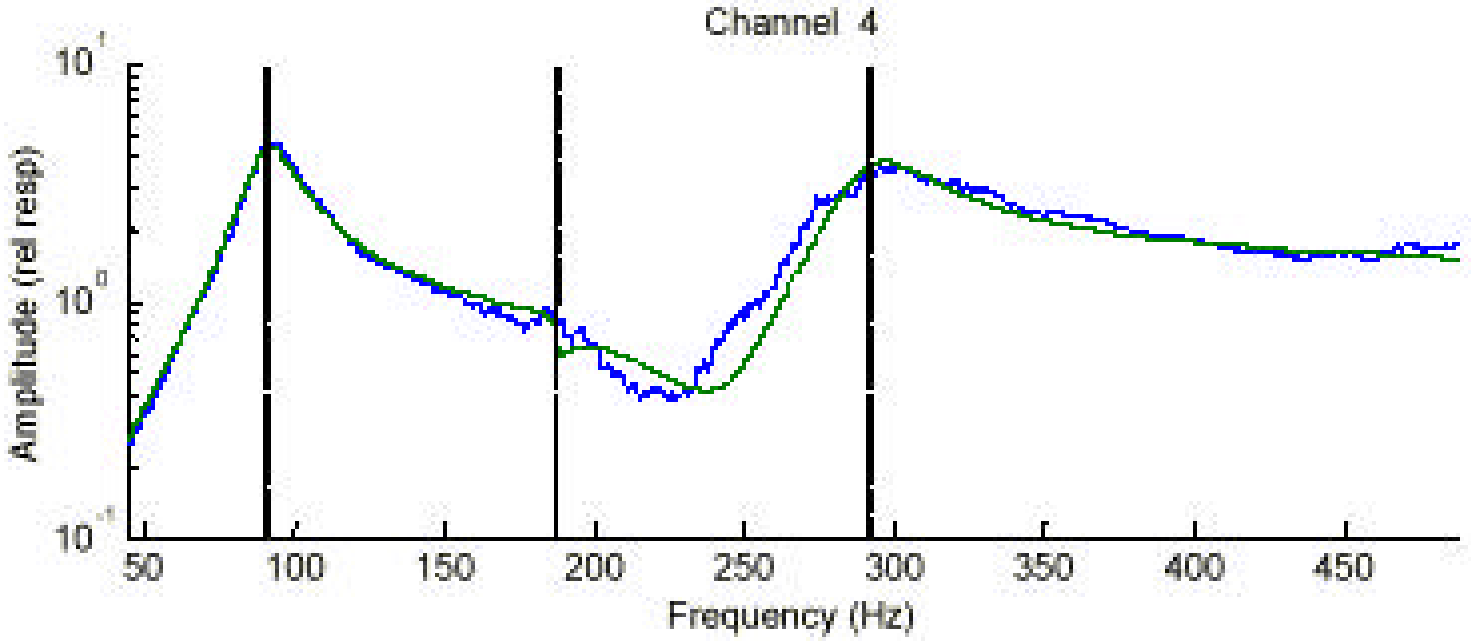


Random Transverse Vibration



Horizontal transverse transfer functions:
-logs do not strike side walls
-fundamental frequency ~ 90 Hz
-middle layers move more
-> 600Hz features due to fixture

Modal Analysis



Blue line is Experimental Transfer function and green line is estimated transfer function

Modal Analysis Results

Mode	MATLAB	Experimental		
	Frequency	Frequency	Damping Ratio	Quality Factor
1st Transverse Shear	88.1 Hz	91 Hz	9.3%	5.4
2nd Transverse Shear	172.5 Hz	187 Hz	1.9%	26.3
3rd Transverse Shear	251.2 Hz	292 Hz	6.1%	8.2

Mode	MATLAB	Experimental		
	Frequency	Frequency	Damping Ratio	Quality Factor
1st Vertical (Accordion)	305.4 Hz	218.5 Hz	4.1%	12.2
2nd Vertical (Accordion)	598.9 Hz	524 Hz	1.4%	35.7

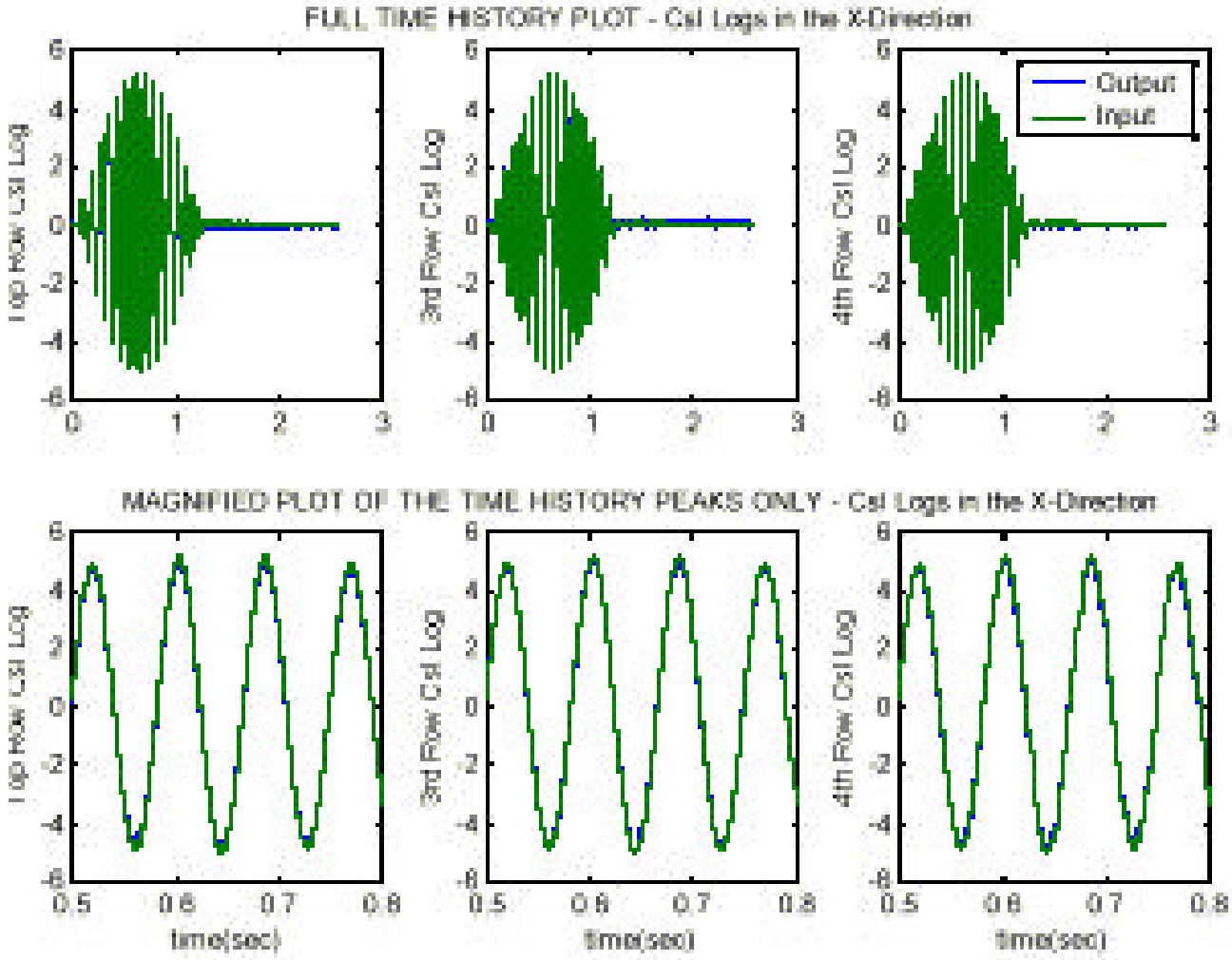
Sine Burst Test

Specification:

Test Axis	Dwell Frequency	Acceleration Level	Duration
Transverse	9.9 Hz	±5.0 $g's_{0\text{-}pk}$	5 cycles
Thrust	12.7 Hz	±8.25 $g's_{0\text{-}pk}$	5 cycles

Goals: -Validate design and workmanship (yes)
-Look for slippage of logs (no slippage)
-Check if anything moved (no)

Sine Burst: No Slippage



GLAST Custom PIN diode

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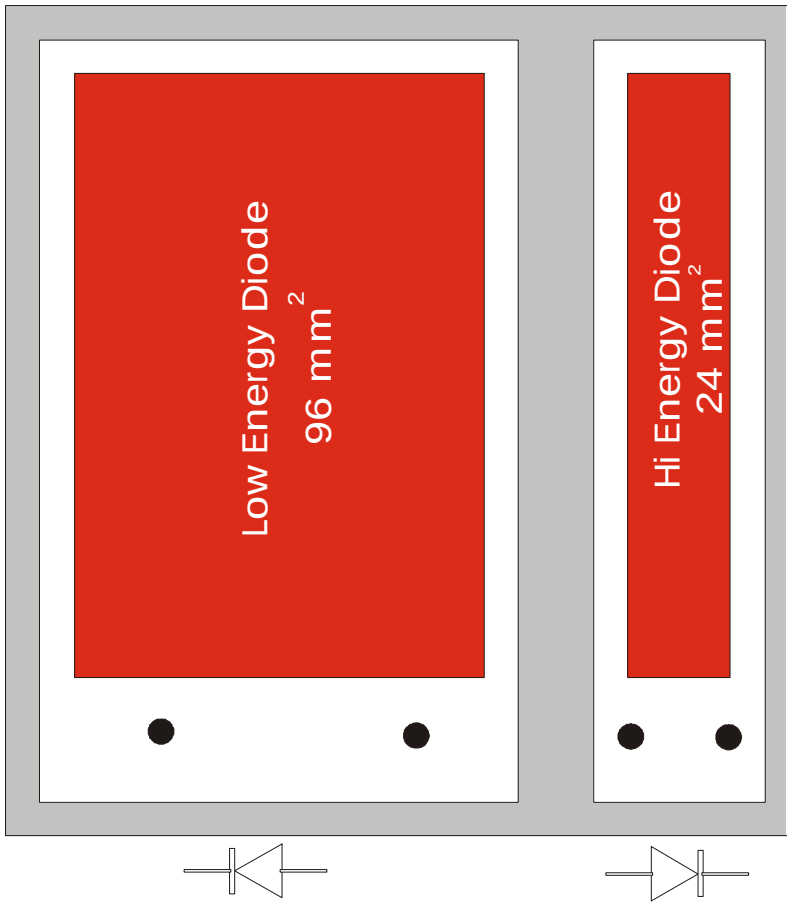
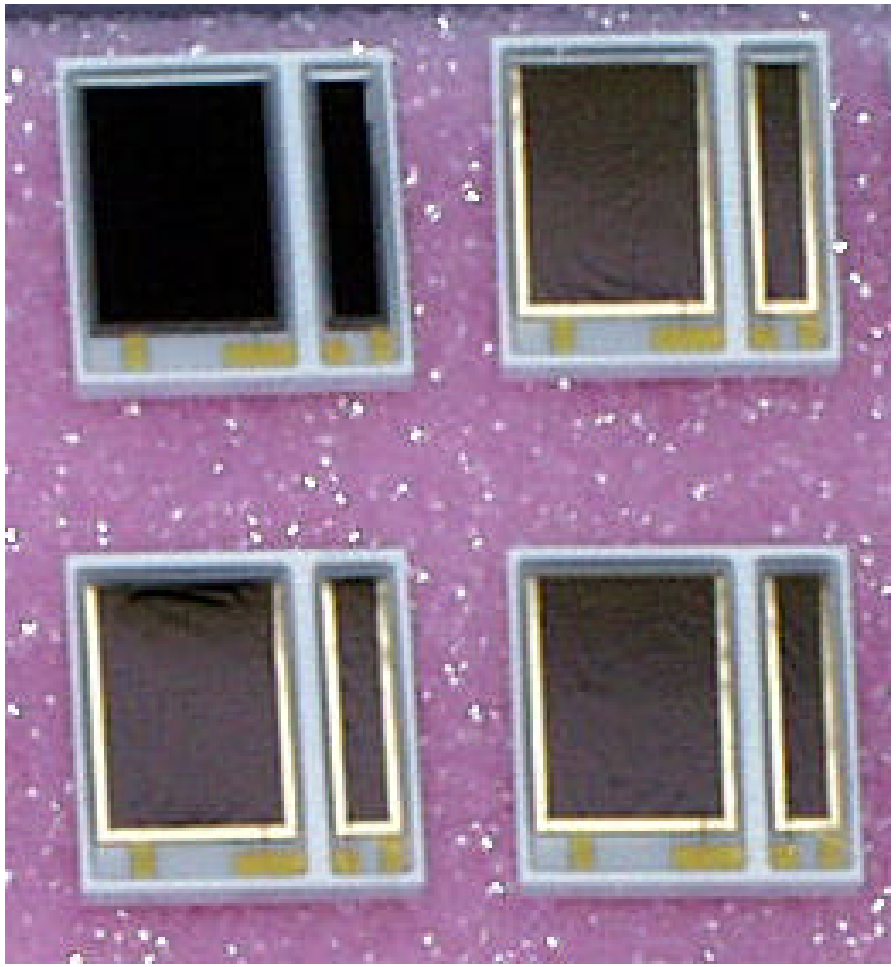
PIN diode Design and Specifications



Front (Optical) Face of PIN

- Two diodes , 96mm^2, 24mm^2
- Single ceramic carrier
- Thin silicon (180 micron)
  (silicon really 280 micron)
- 30V bias
- Large Pin capacitance 75pF mean,
  150pF (90 pF) max
- Small Pin capacitance 20 pF mean,
  40 pF (25 pF) max
- Large Pin dark current 1.5 nA mean,
  5nA max
- Small Pin dark current 0.5 nA mean,
  1.5 nA max

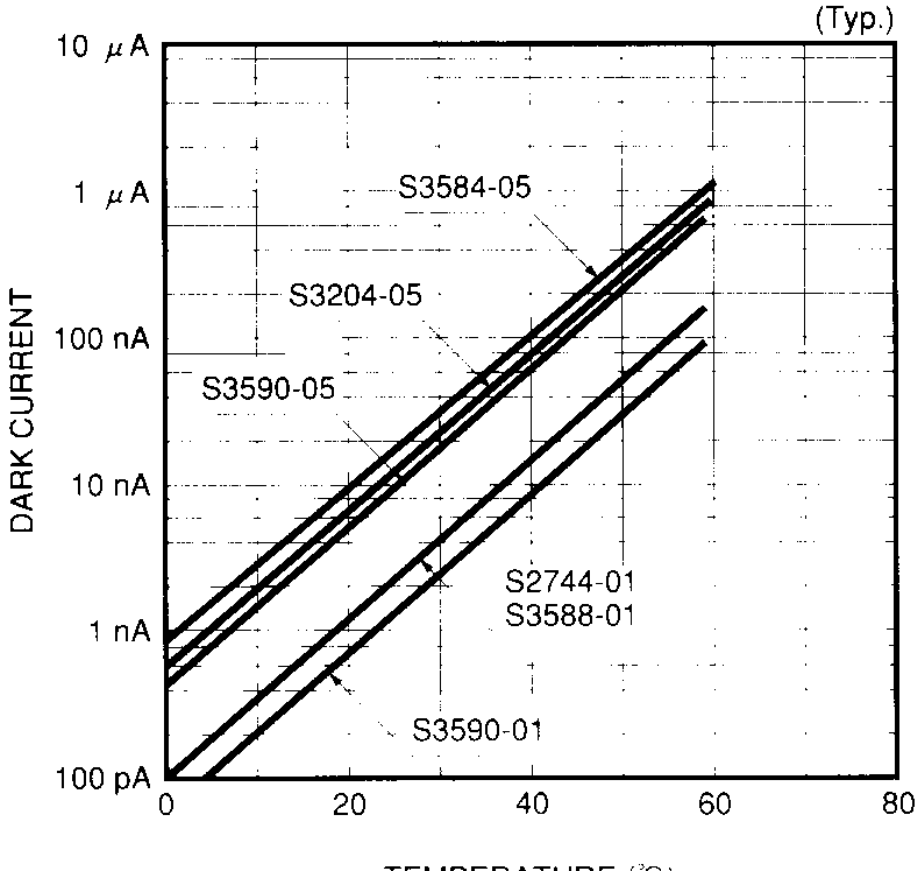
Manufactured Diodes



Pin diode performance:

- mechanically to spec.
- 40 v operation
- Large Pin capacitance mean 66.6 pF,
  range: 65.7 pF to 67.0 pF
- Small Pin capacitance mean 21 pF,
  range: 20.0 pF to 21.8 pF
- Large Pin leakage current 1.5 nA mean,
  range: 0.5 nA to 5 nA
- Small Pin leakage current 0.7 nA mean,
  range: 0.2 nA to 1.5 nA

Dark Current vs Temperature



Direct Energy in Diode

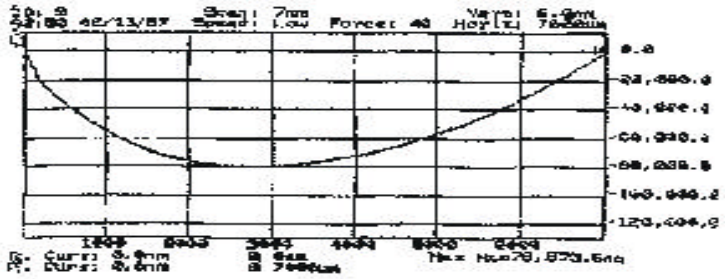
When charged particle crosses Pin diode,
energy is deposited (tracker).

At normal incidence:

- for 180 micron, 42 mg of material,
  => ~ 80 keV deposited
- create ~ 22 000 electrons
- interpreted as ~ 7 MeV in CsI
- most likely relevant at ~ 45 degrees
  => looks like ~ 10 MeV in CsI
- comparable to energy deposited in CsI
  (if in middle of diode)

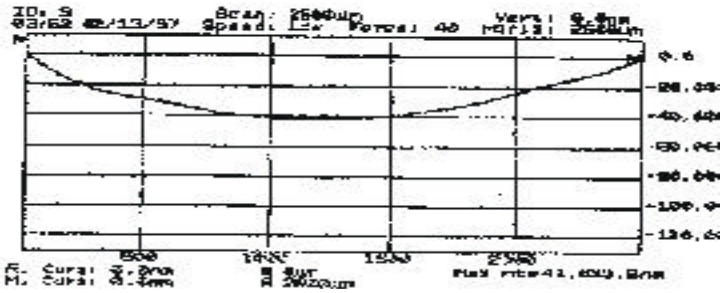
Pin diode surface

Italian



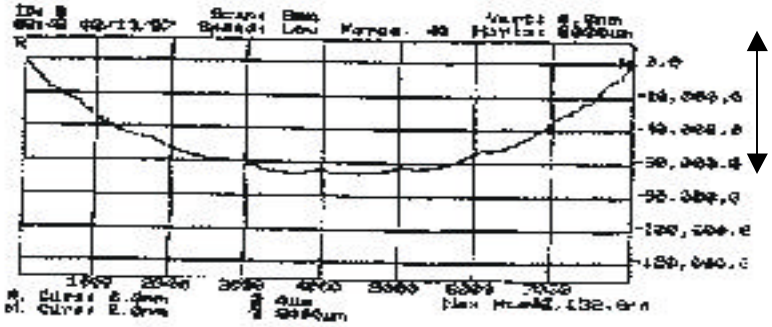
80 μm

Small



40 μm

Large



70 μm

Diode surface is not flat:
- the ceramic well is filled with an optically clear material
- when it cures, there is curvature
- this must be filled with epoxy
- epoxy cannot interact with Hamamatsu's coating

-we used Epotek 301

- have noticed reaction on crystal side

=> probably need thicker layer of epoxy

-need to account for temperature gradients for flight (50 degree C)

-should consider Sylgard

-we did not use it because it did not stick to CsI as well